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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/928,988	08/15/2001	Jun Koyama	740756-2348	8058

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EXAMINER	
NGUYEN, CHANH DUY	

ART UNIT	PAPER NUMBER
2675	

DATE MAILED: 10/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/928,988	KOYAMA ET AL.	
	Examiner	Art Unit	
	Chanh Nguyen	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 12-42* is/are pending in the application.

4a) Of the above claim(s) *7-9,13 and 16-29* is/are withdrawn from consideration.

5)☒ Claim(s) *30-42* is/are allowed.

6)☒ Claim(s) *1-6,10,12,14 and 15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment filed on July 27, 2005 have been entered and considered by examiner.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art (Figures 2-6 and 12B) n view of Yamazaki (U.S. Patent No. 6,175,395 B1).

As to claim 5, Applicant's admitted prior art discloses a semiconductor device including a substrate having at least one driving circuit (see Fig 5B; driver circuit TFT) comprising a plurality of thin film transistors (i.e. gate 407 with source and drain 417 formed one transistor and gate 408 with source and drain 414 formed another transistor) (see Figures 4A-4A and 5A-5B).

Applicant's admitted prior art teaches clock lines (501-506) for supplying clock signals to the driving circuit (201), and wiring lines crossing the clock lines (see Figure 6). Applicant's admitted prior art does not mention black matrices over the thin film transistors. Yamazaki teaches that (1) "an object of the present invention is to form a black matrix on TFTs of a driver circuit" (see column 2, lines 23-25) , (2) "**if the clock line** or the like of a driver circuit **has a wiring line**..."(see column 1, lines 54-57) and (3) "the film is patterned by a known photolithography technique to **form a black matrix 127 on all the wirings** and the TFTs 99 and 100" (column 7,lines 24-26) . It is clear that Yamazaki wiring lines cross the clock lines, and a black matrix (127) formed over the driver circuit region wherein said wiring lines comprises the same layer as the black matrices (see column 2, lines 23-25,lines 63-65, column 3, lines 24-25, column 7,lines 17-36).

It would have been obvious to one of ordinary skill in the art at the invention was made to have used the black matrix as taught by Yamazaki to on the driving circuit wiring of prior art admitted by applicant since the black matrix can of Yamazaki can shield the light for both driving circuit and driver circuits (see column 2,lines 38-50 of Yamazaki).

As to claim 1, Applicant's admitted prior art (Figures 5-6 and 12B) discloses the subject mater of the claim 1 including thin film transistor, clock lines, two layer structures and the lower layer extends in a same direction as the upper layer as recited in the claims wit exception of describing the limitation "wherein said wiring line formed the upper layer is connected to the upper layer".

For example, Figures 5A-5B of the prior art show the a driving circuit TFT which includes clock input terminals 208-209 in Figure 2 as well as clock input terminals 501-509 in Figure 6) formed in the same layers structure as a pixel TFT which includes gate, drain source (Figure 5B). Figure 6 further describes that "in the a driving circuit of a conventional liquid crystal display device, where clock wiring lines, video signal wiring lines, and control wiring lines of a shift register are formed, those wiring lines are formed at the same time a source and drain electrodes of a thin film transistor" (see page 5 line 24 through page 6, line 10 of the specification). Figures 4A- 4D clearly show at least two layers structure for forming source/drain and gate line electrodes. Figure 5A-5B show the wiring lines including clock lines (driver circuit TFT) associated with layers structure of source/drain gate line electrodes (i.e. pixel TFT). Furthermore, Figure 12B details of Figures 5A-5B how the clock lines or each of base portions of the clock lines is made of a two layer structure, a lower layer of the two layer structure comprising the same wiring material as gate electrodes of thin film transistors and , an upper layer of the two layer structure comprising the same wiring material as source and drain electrodes of the thin film transistors. For example, the clock wiring lines are made of two layers: a lower layer (1114) is a gate electrode and an upper layer (1111,

1112) is a source and drain electrode. The lower layer (gate 1114) extends in a direction as the upper layer (see Fig. 12B).

Yamazaki teaches that (1) "an object of the pesent invention is to form a black matrix on TFTs of a driver circuit" (see column 2, lines 23-25) , (2) "**if the clock line** or the like of a driver circuit **has a wiring line**..."(see column 1, lines 54-57) . It is clear that Yamazaki wiring lines (119) formed over the upper layer (i.e. source and drain 117) and connected to the upper layer (i.e. source layer 117). The limitation wiring line is so broad that it can even read on the wiring line (419) of the prior art admitted by applicant. Moreover, if applicant try to claim the wire line as a black matrix (1101) disclosed in Figure 12A of the invention, then Yamazaki also teaches the black matrix (538) formed over upper (source and drain 518 and 522) and connected to the upper layer (source and drain 518 and 522) as shown in Figure 6D.

As to claim 2, Prior Art (Fig.6) clearly teaches an interval between adjacent ones of the clock lines ((e.g., distance between clock lines 501 and 506) being wider than a width of each of the clock lines (i.e., either clock line 501 or 506).

As to claim 3, Prior Art (Figure 2) teaches clock lines (208, 209) being connected to a shift register circuit (216) in the driving circuit (201).

As to claim 4, Prior Art (Figure 2) clearly teaches a pixel portion (224, 226) including a plurality of thin film transistors 226) on said substrate.

As to claim 6, Applicant's admitted prior art clearly teaches each of clock lines or each of base portions of the clock lines is made of a two layer structure, a lower layer of the two layer structure comprising the same wiring material as gate electrodes of

thin film transistors and , an upper layer of the two layer structure comprising the same wiring material as source and drain electrodes of the thin film transistors wherein the lower layer extends in a same direction as the upper layer. That is Figures 5A-5B show the a driving circuit TFT (which includes clock input terminals 208-209 in Figure 2 as well as clock input terminals 501-509 in Figure 6) formed in the same layers structure as a pixel TFT which includes gate, drain source (Figure 5B). Figure 6 further describes that "in the a driving circuit of a conventional liquid crystal display device, where clock wiring lines, video signal wiring lines, and control wiring lines of a shift register are formed, those wiring lines are formed at the same time a source and drain electrodes of a thin film transistor" (see page 5 line 24 through page 6, line 10 of the specification). Figures 4A- 4D clearly show at least two layers structure for forming source/drain and gate line electrodes. Figure 5A-5B show the wiring lines including clock lines (driver circuit TFT) associated with layers structure of source/drain gate line electrodes (i.e. pixel TFT). Furthermore, Figure 12B details of Figures 5A-5B how the clock lines or each of base portions of the clock lines is made of a two layer structure, a lower layer of the two layer structure comprising the same wiring material as gate electrodes of thin film transistors and , an upper layer of the two layer structure comprising the same wiring material as source and drain electrodes of the thin film transistors. For example, the clock wiring lines are made of two layers: a lower layer (1114) is a gate electrode and an upper layer (1111, 1112) is a source and drain electrode. The lower layer (gate 1114) extends in a direction as the upper layer (111, 112) (see Fig. 12B). Even Fig.4A-4D show more clearly the source /drain (414-417)

extending in the same direction as the gate layer (i.e. perpendicular to the paper plane).

5. Claims 10, 12 and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art in view of Mitra (U.S. Patent No. 5,994,765).

As to claim 10, note the discussion of prior art above, prior art admitted by applicant discloses a semiconductor as recited in claim 10 with exception that the prior art does not mention shielding line. For example, Applicant's admitted prior art discloses a semiconductor device including a substrate having at least one driving circuit (see Fig 5B; driver circuit TFT) comprising a plurality of thin film transistors (i.e. gate 407 with source and drain 417 formed one transistor and gate 408 with source and drain 414 formed another transistor) (see Figures 4A-4A and 5A-5B).

Applicant's admitted prior art teaches clock lines (501-506) for supplying clock signals to the driving circuit (201). Figure 6 of the prior art further describes that "in the a driving circuit of a conventional liquid crystal display device, where clock wiring lines, video signal wiring lines, and control wiring lines of a shift register are formed, those wiring lines are formed at the same time a source and drain electrodes of a thin film transistor" (see page 5 line 24 through page 6, line 10 of the specification). Figures 4A- 4D clearly show at least two layers structure for forming source/drain and gate line electrodes. Figure 5A-5B show the wiring lines including clock lines (driver circuit TFT) associated with layers structure of source/drain gate line electrodes (i.e. pixel TFT). Furthermore, Figure 12B details of Figures 5A-5B how the clock lines or each of base

portions of the clock lines is made of a two layer structure, a lower layer of the two layer structure comprising the same wiring material as gate electrodes of thin film transistors and , an upper layer of the two layer structure comprising the same wiring material as source and drain electrodes of the thin film transistors. For example, the clock wiring lines are made of two layers: a lower layer (1114) is a gate electrode and an upper layer (1111, 1112) is a source and drain electrode. The lower layer (gate 1114) extends in a direction as the upper layer (see Fig. 12B).

Mitra teaches a well-known shielding line (103) disposed on interval between the clock lines (101). Therefore, it would have been obvious to one of ordinary skill in the art at the invention was made to have used shielding line as taught by Mitra to the semiconductor of the prior art so as to help prevent clock signals propagated on the clock line from electromagnetically coupling with other signal lines (see column 2, lines 18-22 of Mitra).

As to claims 12 and 14-15, the limitations recited in these claims are met by the prior art admitted by applicant (Figures 5-6 and 12B). For example, the black matrices is known in the art as previously discussed with respect to claim 5. Prior Art (Fig.6) clearly teaches an interval between adjacent ones of the clock lines ((e.g., distance between clock lines 501 and 506) being wider than a width of each of the clock lines (i.e., either clock line 501 or 506) as recited in claim 13. Prior Art (Figure 2) teaches clock lines (208, 209) being connected to a shift register circuit (216) in the driving circuit (201) as recited in claim 14. Prior Art (Figure 2) clearly teaches a pixel portion (224, 226) including a plurality of thin film transistors 226) on said substrate.

Allowable Subject Matter

6. Claims 30-42 are allowed.

,Response to Arguments

7. Applicant's arguments with respect to claims 1-4 have been considered but are moot in view of the new ground(s) of rejection.

In view of amendment, the reference of Yamazaki has been added to claims 1-4 for new ground rejection.

On page 11, second paragraph, applicant argues that "the Official Action appears to misinterpret or misunderstand Figure 12B. Figure 12B shows a cross-sectional view of gate electrode wiring line 1114, which is a lower layer and which extends in a direction parallel to a plane of the page, and a cross-sectional view of source electrodes 1111 and 11122, which are upper layers and which extend in a direction perpendicular to the plane of the page". Examiner disagrees with applicant this point of view since the way to fabricate TFT in the driver circuit having source, drain and gate describes in Figure 4A-4D and 5A-5B. The gate layers (407-408) extends the same direction as source and drain layers (i.e. in a direction perpendicular to the plane of the page). Thus, there is no reason that the gate layer (1104) in Figure 12B extending different direction from source layer (1111, 1112).

On page 11, third paragraph Applicant argues that " Figure 6 shows a line (not numbered) connected to clock line 501 , which corresponds to gate electrode wiring line 1114 of Figure 12B, and clock line 502 itself corresponds to source electrode 1 112 of

Figure 12B. The clock line 502 crosses over the (not numbered) connected to clock line 501. Similarly, source electrode (upper layer) 1112 crosses over gate electrode wiring line (lower layer) 1114 in Figure 12B. Therefore, source electrode (upper layer) 1112 extends in a different direction than gate electrode wiring line (lower layer) 1114". However, Figure 6 does not describe where is the source, drain or gate are located.. The clock lines (501 and 502) does not correspond to gate nor source/drain as applicant argument. The clock lines is the clock line. The clock line cannot be a source /drain or gate. Precisely, the clock line can be integrated with TFT having source, drain and gate, but the clock line can not substituted as source, drain or gate. Figure 4A-4D and 5A-5B clearly show both source/drain I (414, 417) and gate layer (407, 408) extending the same direction each other. This TFT is integrated with the clock line (501, 506) , video line , power line (507, 508) to form a driver circuit TFT. Figure 12B demonstrated one of the lines (i. E. clock line) is integrated with TFT. Thus the two layers: gate and source/ drain in prior art is clearly extended in the same direction as discloses in Figures 4-5.

On page 12, Applicant argues that " Figures 5, 6 and 12B also do not teach at least one wiring line crossing clock lines and that a wiring line formed over an upper layer is connected to the upper layer,their explicitly or inherent". However, this limitation is met by Yamazaki as set forth in the rejection..

From last paragraph of page 12 to page 14, applicant simply copy the section MPEP 2142-2143.01 and concludes that "there is no suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary

skill in art to combine reference teachings to achieve the claimed invention". Examiner disagrees with applicant this point of view because the teaching, suggestion, or motivation is clearly found in the references of as set forth in the rejection. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Yamazaki recognizes that the light can be shielded both driving circuit and pixel circuit as disclosed in column 2, liens 38-50 of Yamazaki.

On page 15, first paragraph, Applicant argues that the office action has not shown why black matrix 16 or 18 of Figure 12 of Yamazaki should be combine with structure shown in Figure 5, 6 , 12B. However, Yamazaki recognizes the problem of forming black matrix on the pixel electrode (i.e. the prior art admitted by applicant does) would increase the power consumption (see column 2, lines 8-17). Thus, in order to reduce the power consumption, Yamazaki teaches forming the black matrix on TFTs of the driver circuit (see column 2, lines 23-26).

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chanh Nguyen whose telephone number is (571) 272-7772. The examiner can normally be reached on Monday- Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chanh Nguyen
Primary Examiner
Art Unit 2675

CN

C. Nguyen
October 16, 2005